

What is claimed is:

1. A semiconductor memory device comprising:

a sense amplifier array unit including a plurality of
5 bit-line sense amplifiers arrayed to each other;

a first driver, located at one side of the sense
amplifier array unit, for generating a driving voltage of the
plurality of bit-line sense amplifiers;

a second driver, located at the other side of the sense
10 amplifier array unit, for producing the driving voltage of the
plurality of bit-line sense amplifiers;

a first power line, which is connected between an output
node of the first driver and that of the second driver, and to
which a driving voltage input node of each of the plurality of
15 bit-line sense amplifiers is attached in parallel; and

a second power line, connected to the first power line in
parallel between the output node of the first driver and that
of the second driver, and strapped with the first power line
at least one point.

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2. The semiconductor memory device as recited in claim 1,
wherein the strapping of the first power line and the second
power line is implemented at a central region of the sense
amplifier array unit.

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3. A semiconductor memory device comprising:

a sense amplifier array unit including a plurality of

bit-line sense amplifiers arrayed to each other, wherein each of the plurality of bit-line sense amplifiers has a first driving voltage input node being a pull-up source and a second driving voltage input node being a pull-down source of bit lines;

a first driver, located at one side of the sense amplifier array unit, for generating a first and a second driving voltage of the plurality of bit-line sense amplifiers;

a second driver, located at the other side of the sense amplifier array unit, for producing the first and the second driving voltages of the plurality of bit-line sense amplifiers;

a first power line, which is connected between a first driving voltage output node of the first driver and that of the second driver, and to which a first driving voltage input node of each of the plurality of bit-line sense amplifiers is attached in parallel;

a second power line, connected to the first power line in parallel between the first driving voltage output node of the first driver and that of the second driver, and strapped with the first power line at least one point;

a third power line, which is connected between a second driving voltage output node of the first driver and that of the second driver, and to which a second driving voltage input node of said each of the plurality of bit-line sense amplifiers is attached in parallel; and

a fourth power line, connected to the third power line in

parallel between the second driving voltage output node of the first driver and that of the second driver, and strapped with the third power line at least one point.

5 4. The semiconductor memory device as recited in claim 3, wherein the strapping of the third power line and the fourth power line is implemented at a central region of the sense amplifier array unit.

10 5. The semiconductor memory device as recited in claim 3, wherein each of the first driver or the second driver includes:

 a pull-up means for providing an internally generated voltage to the first driving voltage output node under the
15 control of a control signal;

 a pull-down means for pulling down the second driving voltage output node to a ground level by simultaneously actuated with the pull-up means; and

 a pre-charging means for pre-charging the first driving
20 voltage output node and the second driving voltage output node with a pre-charge voltage when the pull-up means and the pull-down means are inactivated.

 6. The semiconductor memory device as recited in claim 5,
25 wherein the pull-up means is constructed with a PMOS transistor and the pull-down means is formed with an NMOS transistor.

7. The semiconductor memory device as recited in claim 3, wherein each of the first driver or the second driver includes:

a first pull-up means for supplying an external voltage to the first driving voltage output node under the control of a first control signal;

a second pull-up means for providing an internally generated voltage to the first driving voltage output node in response to a second control signal;

a pull-down means for pulling down the second driving voltage output node to a ground level by simultaneously actuated with the first pull-up means; and

a pre-charging means for pre-charging the first driving voltage output node and the second driving voltage output node with a pre-charge voltage when the first and the second pull-up means and the pull-down means are inactivated.

8. The semiconductor memory device as recited in claim 7, wherein the first and the second pull-up means are constructed with PMOS transistors and the pull-down means is formed with an NMOS transistor.

9. The semiconductor memory device as recited in claim 7, wherein the internally generated voltage has a voltage level identical to that of a high data stored at a memory cell.

10. A semiconductor memory device comprising:

a sense amplifier array unit including a plurality of bit-line sense amplifiers arrayed to each other, wherein each bit-line sense amplifier has a first driving voltage input node being a pull-up source and a second driving voltage input node being a pull-down source of bit-lines;

a first driver, located at one side of the sense amplifier array unit, for generating a first and a second driving voltage of the plurality of bit-line sense amplifiers;

a second driver, located at the other side of the sense amplifier array unit, for producing the first and the second driving voltages of the plurality of bit-line sense amplifiers;

a third driver, located at one side of a memory cell block, for generating the first and the second driving voltages of the plurality of bit-line sense amplifiers;

a fourth driver, located at the other side of the memory cell block, for producing the first and the second driving voltages of the plurality of bit-line sense amplifiers;

a first power line, which is connected between a first driving voltage output node of the first driver and that of the second driver, and to which a first driving voltage input node of each of the plurality of bit-line sense amplifiers is attached in parallel;

a second power line, connected to the first power line in parallel between a first driving voltage output node of the third driver and that of the fourth driver, and strapped with the first power line at least one point;

a third power line, which is connected between a second driving voltage output node of the first driver and that of the second driver, and to which a second driving voltage input node of said each of the plurality of bit-line sense amplifiers is attached in parallel; and

a fourth power line, connected to the third power line in parallel between a second driving voltage output node of the third driver and that of the fourth driver, and strapped with the third power line at least one point.

11. The semiconductor memory device as recited in claim 10, wherein each of the first to the fourth drivers includes:

a pull-up means for providing an internally generated voltage to the first driving voltage output node under the control of a control signal;

a pull-down means for pulling down the second driving voltage output node to a ground level as simultaneously actuated with the pull-up means; and

a pre-charging means for pre-charging the first driving voltage output node and the second driving voltage output node with a pre-charge voltage when the pull-up means and the pull-down means are inactivated.

12. The semiconductor memory device as recited in claim 10, wherein each of the first to the fourth drivers includes:

a first pull-up means for supplying an external voltage to the first driving voltage output node under the control of

a first control signal;

a second pull-up means for providing an internally generated voltage to the first driving voltage output node in response to a second control signal;

5 a pull-down means for pulling down the second driving voltage output node to a ground level as simultaneously actuated with the first pull-up means; and

a pre-charging means for pre-charging the first driving voltage output node and the second driving voltage output node
10 with a pre-charge voltage when the first and the second pull-up means and the pull-down means are inactivated.

13. A semiconductor memory device comprising:

a sense amplifier array unit including a plurality of
15 bit-line sense amplifiers arrayed to each other;

a driver, located at one side of the sense amplifier array unit, for generating a driving voltage of the plurality of bit-line sense amplifiers;

a first power line, which is connected to an output node
20 of the driver, and to which a driving voltage input node of each of the plurality of bit-line sense amplifiers is attached in parallel; and

a second power line, connected to the first power line in parallel at the output node of the driver, and strapped with
25 the first power line at least one point.

14. A semiconductor memory device comprising:

a sense amplifier array unit including a plurality of bit-line sense amplifiers arrayed to each other, wherein each bit-line sense amplifier has a first driving voltage input node being a pull-up source and a second driving voltage input node being a pull-down source of bit lines;

a driver, located at one side of the sense amplifier array unit, for generating a first and a second driving voltage of the plurality of bit-line sense amplifiers;

a first power line, which is connected to a first driving voltage output node of the driver, and to which a first driving voltage input node of each of the plurality of bit-line sense amplifiers is attached in parallel;

a second power line, connected to the driving voltage output node of the driver, and strapped with the first power line at least one point;

a third power line, which is connected to a second driving voltage output node of the driver, and to which a second driving voltage input node of said each of the plurality of bit-line sense amplifiers is attached in parallel; and

a fourth power line, connected to the second driving voltage output node of the driver, and strapped with the third power line at least one point.